

# CORSAIR

2048 MB DDR2 Server Memory Module

# CM72DD2048R-XXX

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## Key Features

- ◆ 240-pin, dual in-line memory module (DIMM)
- ◆ Ultra high density using 1 GBit SDRAM devices
- ◆ ECC 1-bit error detection and correction
- ◆ Registered inputs with one-clock delay
- ◆ Phase-locked loop (PLL) clock driver to reduce loading
- ◆ 256 MB x 72
- ◆ JEDEC standard 1.8V I/O (SSTL\_18-compatible)
- ◆ Four-bit prefetch architecture
- ◆ Off-chip driver (OCD) impedance calibration
- ◆ On-die termination (ODT)
- ◆ Low profile (1.2"), ideal for 1U rack mount servers

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## Selection Guide

# CM72DD2048R-XXX

MODULE SIZE:  
2048 MByte

SPEED:

667: DDR2-667 (667 MB/s)

400: DDR2-400 (400 MB/s)

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**General Description**

The CM72DD2048R is a DDR2 Dual Inline Memory Module (DIMM), designed for applications in which both performance and density are critical. This DIMM includes Error Checking and Correcting (ECC) for maximum reliability, and has registered address and control signals to enable fully configured systems. These modules are constructed using 1 GBit SDRAMs, and are fully compliant with JEDEC specifications.

These DIMMs are constructed using 128MBx8 SDRAMs in BGA packages. The module also includes an EEPROM to support Serial Presence Detect (SPD) requirements. Decoupling capacitors are mounted on the printed circuit board for each SDRAM device, and On-Die Termination is provided on all lines. The synchronous design of these Corsair SDRAM DIMMs allows precise cycle control with the use of the system clock. I/O transactions are possible on every clock cycle. The high clock frequency and high density of this device enable a high level of performance to be achieved in advanced workstations and servers.

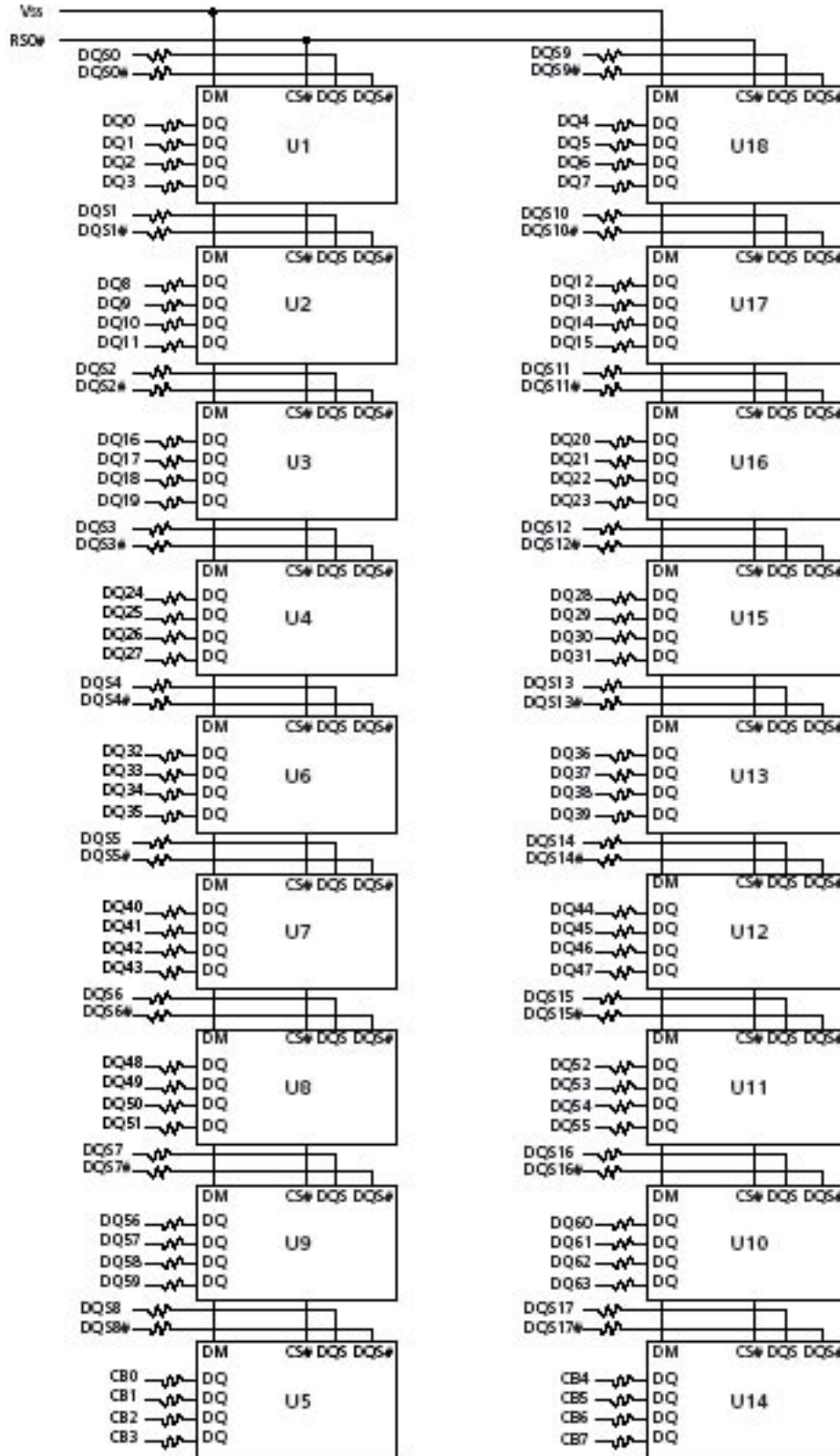
**Pin Definitions**

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
73, 74, 192	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
71, 190	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
57, 58, 60, 61, 63, 70, 176, 177, 179, 180, 182, 183, 188	A0-A12 (512MB), A0-A13 (1GB)	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for Read/Write commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the opcode during a LOAD MODE command.

### Pin Configuration

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
3, 4, 9, 10, 12, 13, 21, 22, 24, 25, 30, 21, 33, 34, 39, 40, 80, 81, 86, 87, 89, 90, 95, 96, 98, 99, 107, 708, 110, 111, 116, 117, 122, 123, 128, 129, 131, 132, 140, 141, 143, 144, 149, 150, 152, 153, 158, 159, 199, 200, 205, 206, 208, 209, 214, 215, 217, 218, 226, 227, 229, 230, 235, 236	DQ0-DQ63	I/O	Data Input/Output: Bidirectional data bus.
6, 7, 15, 16, 27, 28, 36, 37, 45, 46, 83, 84, 92, 93, 104, 105, 113, 114, 125, 126, 134, 135, 146, 147, 155, 156, 164, 165, 202, 203, 211, 212, 223, 224, 232, 233	DQS0-DQS17, DQS0#-DQS17#	I/O	Data Strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
42, 43, 48, 49, 161, 162, 167, 168	CB0-CB7	I/O	Check Bits: ECC, 1-bit error detection and correction.
120	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect device.
101, 239, 240	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
119	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
18	RESET#	Input	Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.
53, 59, 64, 67, 69, 172, 178, 184, 187, 189, 197	VDD	Supply	Power Supply: 1.8V +/-0.1V
51, 56, 62, 72, 75, 78, 170, 175, 181, 191, 194	VDDQ	Supply	DQ Power Supply: 1.8V +/-0.1V. Isolated on the device for improved noise immunity.
1	VREF	Supply	SSTL_18 reference voltage.
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 65, 66, 79, 82, 85, 88, 91, 94, 97, 100, 103, 106, 108, 112, 115, 118, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 169, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237	VSS	Supply	Ground.
238	VDDSPD	Supply	Serial EEPROM positive power supply: +1.7V to +3.6V.
19, 54 (512MB, 1GB), 55, 68, 76, 77, 102, 171, 196 (512MB), 173, 174	NC	-	No Connect: These pins should be left unconnected.
137, 138, 220, 221	RFU	-	Reserved for Future Use

Functional Block Diagram



### DC Electrical Specifications

#### Absolute Maximum DC Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS	
VDD	VDD Supply Voltage Relative to TSS	-1	2.3	V	
VDDQ	VDDQ Supply Voltage Relative to VSS	-0.5	2.3	V	
VDDL	VDDL Supply Voltage Relative to VSS	-0.5	2.3	V	
VIN, VOUT	Voltage on any Pin Relative to VSS	-0.5	2.3	V	
TSTG	Storage Temperature (Tcase)	-55	100	C	
TOPR	Operating Temperature (TOPR) (Ambient)	0	85	C	
II	Input Leakage Current; Any input 0V VIN VDD; VREF input 0V VIN 0.95V; (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE#	-5	5	μA
		S#, CKE			
		CK, CK#			
IQZ	Output Leakage Current; 0V VOUT VDDQ; DQs and ODT are disabled	-5	5	μA	

#### Recommended DC Operative Conditions

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS
VDD	Supply Voltage	1.7	1.8	1.9	V
VDDL	VDDL Supply Voltage	1.7	1.8	1.9	V
VDDQ	I/O Supply Voltage	1.7	1.8	1.9	V
VREF	I/O Reference Voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V
VTT	I/O Termination Voltage (system)	VREF - 40	VREF	VREF + 40	mV

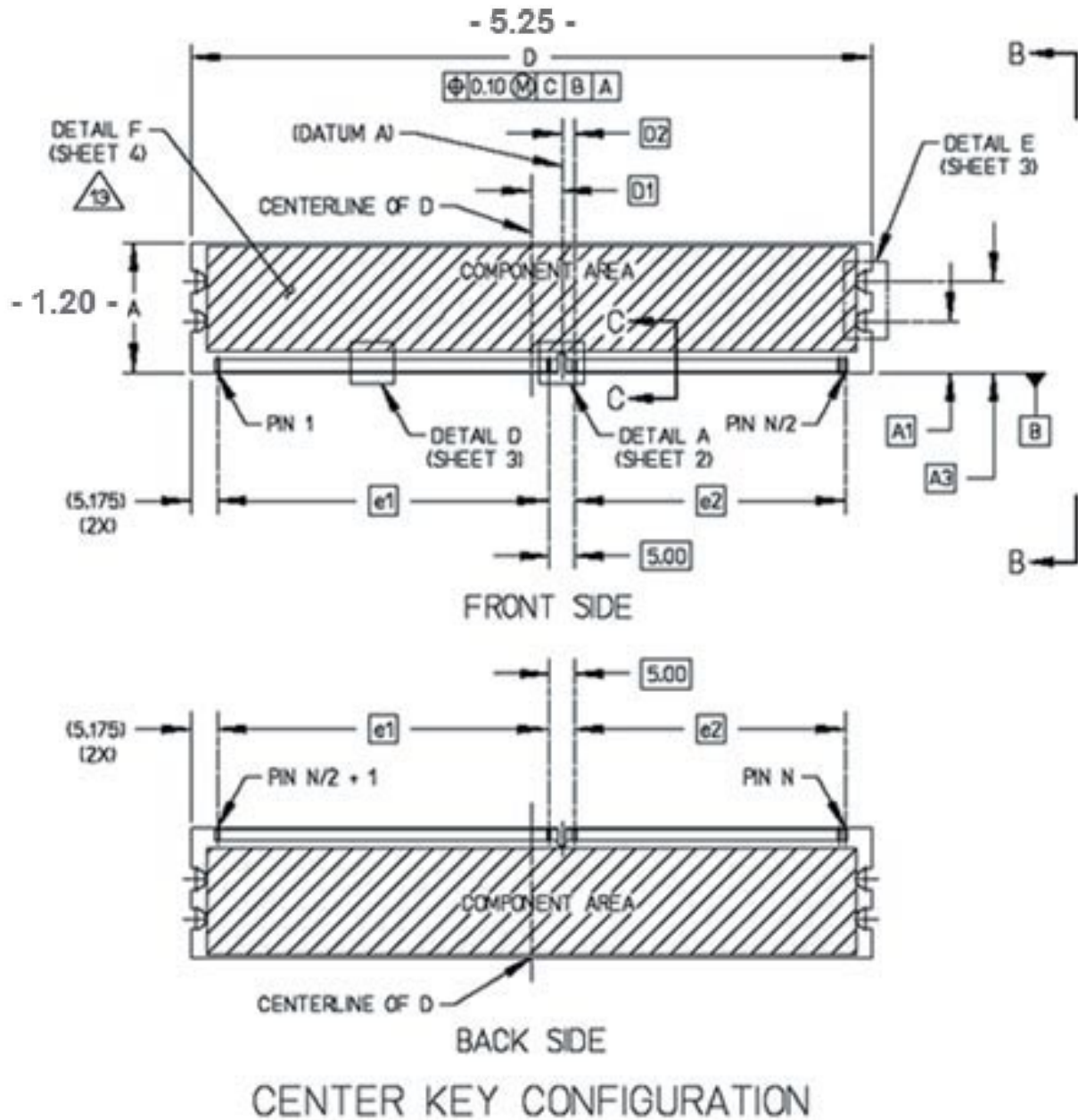
#### Capacitance

SYMBOL	PARAMETER	MIN	MAX	UNITS
CI1	Input Capacitance: CK, CK# (PLL Inputs)	2.0	3.0	pF
CI2	Input Capacitance: BA0, BA1, BA2, A0-A13, S#, RAS#, CAS#, WE#, CKE, ODT (Registered Buffer Inputs)	2.5	4.0	pF
CIO	Input/Output Capacitance: DQ, DQS	2.5	4.0	pF

#### DC Electrical Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS
VDDSPD	Supply Voltage	1.7	3.6	V
VIH	Input High Voltage: Logic 1; All inputs	VDDSPD x 0.7	VDDSPD + 0.5	V
VIL	Input Low Voltage: Logic 0; All inputs	-0.6	VDDSPD x 0.3	V
VOL	Output Low Voltage: IOU = 3mA	-	0.4	V





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