



1024MB Fully Buffered DIMM Server Memory Module

CM72FB1024-XXX

Key Features

- ◆ 240-pin, Fully Buffered dual in-line memory module (FB-DIMM)
- ◆ Ultra high density using 512 MBit SDRAM devices
- ◆ CRC and ECC error detection and correction
- ◆ Advanced Memory Buffer (AMB)
- ◆ 128 MB x 72
- ◆ JEDEC standard 1.5V high speed differential point-to-point link
- ◆ Four-bit prefetch architecture
- ◆ Off-chip driver (OCD) impedance calibration
- ◆ On-die termination (ODT)
- ◆ Low profile (1.2"), ideal for 1U rack mount servers

Selection Guide

CM72FB1024-XXX

MODULE SIZE:
1024 MByte

SPEED (XXX):
533: DDR2-533 (6.3 GB/s)
667: DDR2-667 (8.0 GB/s)



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General Description

The CM72FB1024 is a DDR2 Fully Buffered Dual Inline Memory Module (FB-DIMM), designed for applications in which both performance and density are critical. This DIMM includes Error Checking and Correcting (ECC) for maximum reliability, and has an Advanced Memory Buffer (AMB) for data, address and control signals to enable fully configured systems. These modules are constructed using 512 MBit SDRAMs, and are fully compliant with JEDEC specifications.

These DIMMs are constructed using 64MB x 4 SDRAMs in BGA packages. The module also includes an EEPROM to support Serial Presence Detect (SPD) requirements. Decoupling capacitors are mounted on the printed circuit board for each SDRAM device, and On-Die Termination is provided on all lines. The synchronous design of these Corsair SDRAM DIMMs allows precise cycle control with the use of the system clock. I/O transactions are possible on every clock cycle. The high clock frequency and high density of this device enable a high level of performance to be achieved in advanced workstations and servers.



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Pin Assignment

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VDD	41	PN13#	81	VSS	121	VDD	161	SN13#	201	VSS
2	VDD	42	VSS	82	PS4	122	VDD	162	VSS	202	SS4
3	VDD	43	VSS	83	PS4#	123	VDD	163	VSS	203	SS4#
4	VSS	44	RFU	84	VSS	124	VSS	164	RFU1	204	VSS
5	VDD	45	RFU	85	VSS	125	VDD	165	RFU1	205	VSS
6	VDD	46	VSS	86	RFU1	126	VDD	166	VSS	206	RFU1
7	VDD	47	VSS	87	RFU1	127	VDD	167	VSS	207	RFU1
8	VSS	48	PN12	88	VSS	128	VSS	168	SN12	208	VSS
9	VCC	49	PN12#	89	VSS	129	VCC	169	SN12#	209	VSS
10	VCC	50	VSS	90	PS9	130	VCC	170	VSS	210	SS9
11	VSS	51	PN6	91	PS9#	131	VSS	171	SN6	211	SS9#
12	VCC	52	PN6#	92	VSS	132	VCC	172	SN6#	212	VSS
13	VCC	53	VSS	93	PS5	133	VCC	173	VSS	213	SS5
14	VSS	54	PN7	94	PS5#	134	VSS	174	SN7	214	SS5#
15	VTT	55	PN7#	95	VSS	135	VTT	175	SN7#	215	VSS
16	VID1	56	VSS	96	PS6	136	VID0	176	VSS	216	SS6
17	RESET#	57	PN8	97	PS6#	137	DNU/M_TEST	177	SN8	217	SS6#
18	VSS	58	PN8#	98	VSS	138	VSS	178	SN8#	218	VSS
19	RFU2	59	VSS	99	PS7	139	RFU2	179	VSS	219	SS7
20	RFU2	60	PN9	100	PS7#	140	RFU2	180	SN9	220	SS7#
21	VSS	61	PN9#	101	VSS	141	VSS	181	SN9#	221	VSS
22	PN0	62	VSS	102	PS8	142	SN0	182	VSS	222	SS8
23	PN0#	63	PN10	103	PS8#	143	SN0#	183	SN10	223	SS8#
24	VSS	64	PN10#	104	VSS	144	VSS	184	SN10#	224	VSS
25	PN1	65	VSS	105	RFU2	145	SN1	185	VSS	225	RFU2
26	PN1#	66	PN11	106	RFU2	146	SN1#	186	SN11#	226	RFU2
27	VSS	67	PN11#	107	VSS	147	VSS	187	SN11#	227	VSS
28	PN2	68	VSS	108	VDD	148	SN2	188	VSS	228	SCK
29	PN2#	69	VSS	109	VDD	149	SN2#	189	VSS	229	SCK#
30	VSS	70	PS0	110	VSS	150	VSS	190	SS0	230	VSS
31	PN3	71	PS0#	111	VDD	151	SN3	191	SS0#	231	VDD
32	PN3#	72	VSS	112	VDD	152	SN3#	192	VSS	232	VDD
33	VSS	73	PS1	113	VDD	153	VSS	193	SS1	233	VDD
34	PN4	74	PS1#	114	VSS	154	SN4	194	SS1#	234	VSS
35	PN4#	75	VSS	115	VDD	155	SN4#	195	VSS	235	VDD
36	VSS	76	PS2	116	VDD	156	VSS	196	SS2	236	VDD
37	PN5	77	PS2#	117	VTT	157	SN5	197	SS2#	237	VTT
38	PN5#	78	VSS	118	SA2	158	SN5#	198	VSS	238	VDDSPD
39	VSS	79	PS3	119	SDA	159	VSS	199	SS3	239	SA0
40	PN13	80	PS3#	120	SCL	160	SN13	200	SS3#	240	SA1



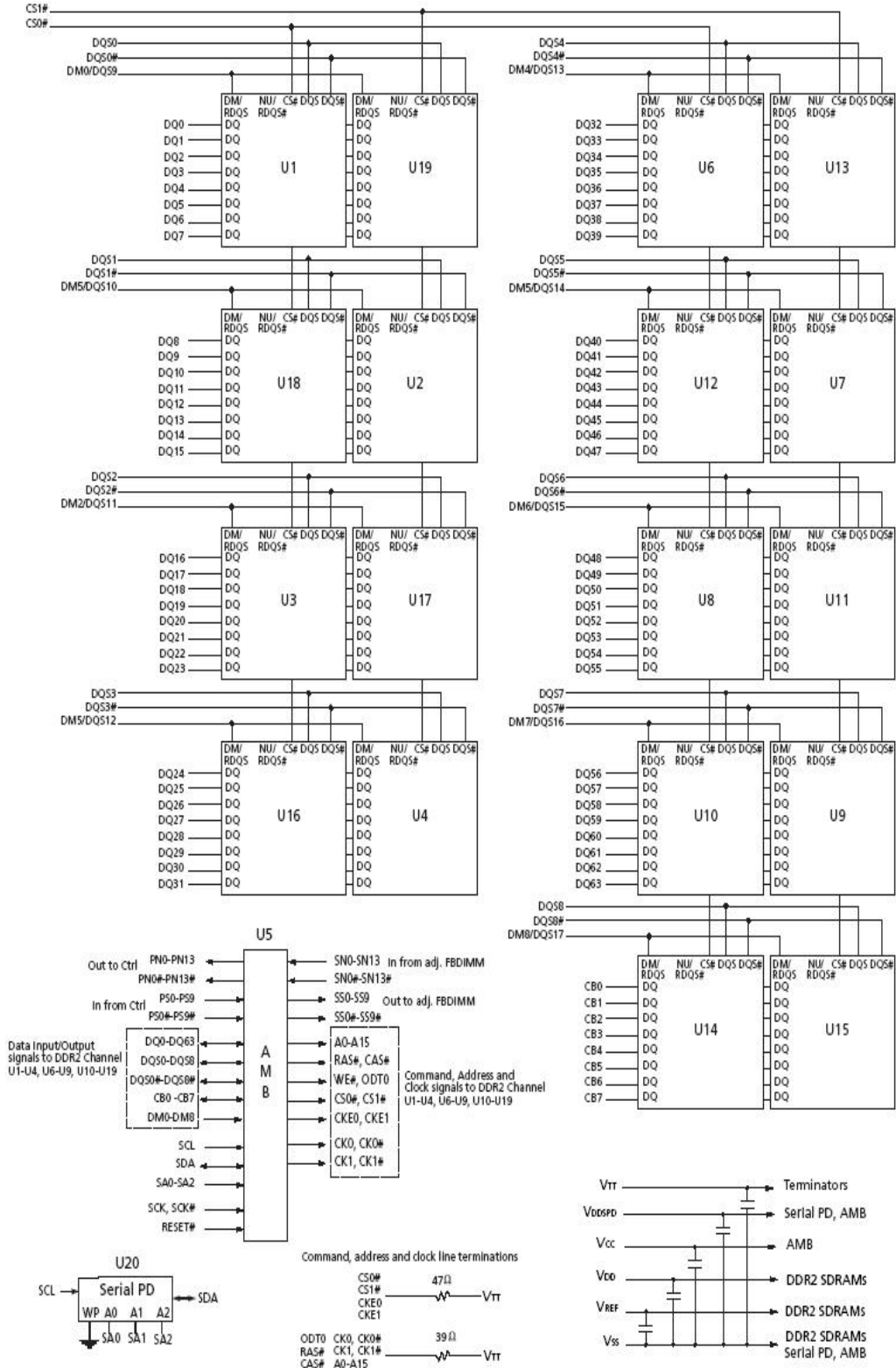
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Pin Description

Pin Name	Pin Description	Count	Note
SCK	System Clock Input, positive line	1	1
/SCK	System Clock Input, negative line	1	1
PN[13:0]	Primary Northbound Data, positive lines	14	
/PN[13:0]	Primary Northbound Data, negative lines	14	
PS[9:0]	Primary Southbound Data, positive lines	10	
/PS[9:0]	Primary Southbound Data, negative lines	10	
SN[13:0]	Secondary Northbound Data, positive lines	14	
/SN[13:0]	Secondary Northbound Data, negative lines	14	
SS[9:0]	Secondary Southbound Data, positive lines	10	
/SS[9:0]	Secondary Southbound Data, negative lines	10	
SCL	Serial Presence Detect (SPD) Clock Input	1	
SDA	SPD Data Input / Output	1	
SA[2:0]	SPD Address Inputs, also used to select the DIMM number in the AMB	3	
VID[1:0]	Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs VID[0] is VDD value: OPEN = 1.8 V, GND = 1.5 V; VID[1] is VCC value: OPEN = 1.5 V, GND = 1.2 V	2	
/RESET	AMB reset signal	1	
RFU	Reserved for Future Use	16	2
VCC	AMB Core Power and AMB Channel Interface Power (1.5 Volt)	8	
VDD	DRAM Power and AMB DRAM I/O Power (1.8 Volt)	24	
VTT	DRAM Address/Command/Clock Termination Power (VDD/2)	4	
VDDSPD	SPD Power	1	
VSS	Ground	80	
DNU/M_Test	The DNU/M_Test pin provides an external connection on R/Cs A-D for testing the margin of Vref which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time.	1	1
	Total	240	

Note: <1> System Clock Signals SCK and SCK switch at one half the DRAM CK/CK frequency.
 <2> Eight pins reserved for forwarded clocks, eight pins reserved for future architecture flexibility.

Block Diagram





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DC Electrical Specifications

Absolute Maximum DC Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS	
VDD	VDD Supply Voltage Relative to VSS	-0.5	2.3	V	
VTT	VTT Supply Voltage Relative to VSS	-0.5	2.3	V	
VCC	VDDL Supply Voltage Relative to VSS	-0.3	1.75	V	
VIN, VOUT	Voltage on any Pin Relative to VSS	-0.3	1.75	V	
TSTG	Storage Temperature (Tcase)	-55	100	C	
TOPR	Operating Temperature DRAM (Tcase)*	0	95	C	
IL	Leakage Current	Link	-5	5	μA
		Reset	-90	90	μA
TOPR	Operating Temperature AMB (Tcase)	0	110	C	

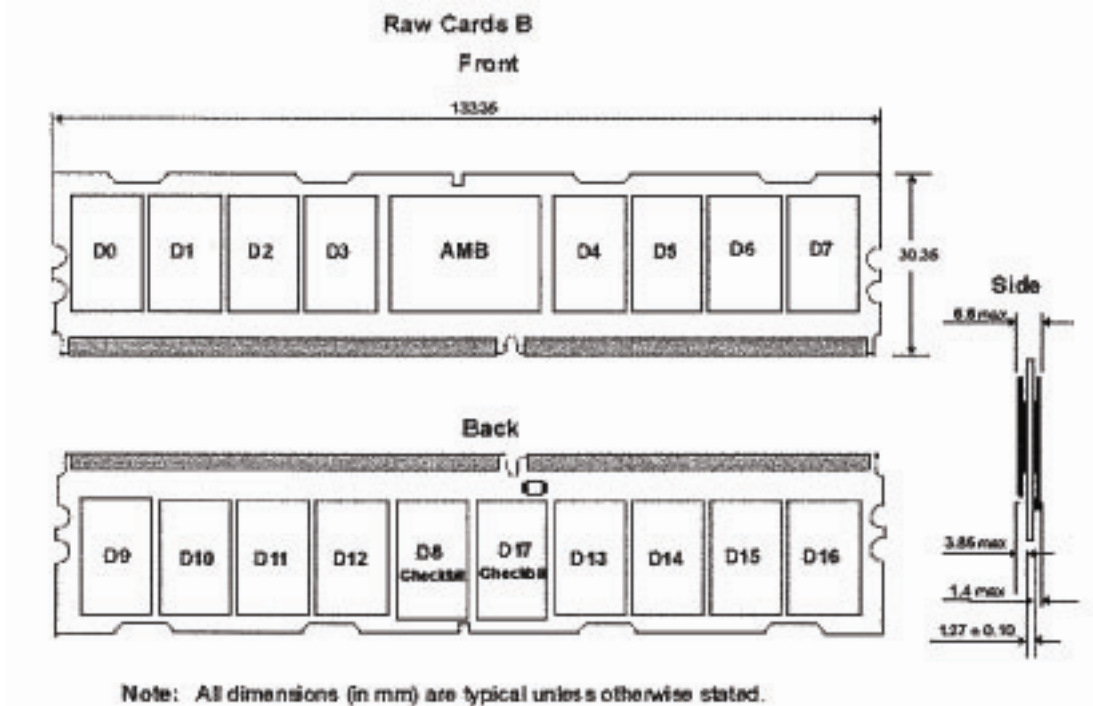
Recommended DC Operative Conditions

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS
VDD	Supply Voltage	1.7	1.8	1.9	V
VCC	AMB Supply Voltage	1.46	1.50	1.54	V
VTT	I/O Termination Voltage (system)	0.48x VDD	0.50 x VDD	0.52 x VDD	V

DC Electrical Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS
VDDSPD	Supply Voltage	3.0	3.6	V
VIH	Input High Voltage: Logic 1; SPD	2.1	VDDSPD	V
VIL	Input Low Voltage: Logic 0; SPD		0.8	V
VOL	Output Low Voltage: IOOUT = 3mA	-	0.4	V

For DRAM case temperature above 85 C, the Auto-Refresh Command interval must be reduced to 3.9us.

Package Information


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