



CM74SD4096RLP

4 GByte Registered DDR DIMM with ECC

Key Features

- ◆ Error Checking and Correcting (ECC) for maximum memory reliability
- ◆ Ultra high density using 1024 MBit SDRAM devices
- ◆ High Performance
 - registered synchronous Double Data Rate SDRAM
 - all inputs synchronized to system clock
 - data transferred on both rising and falling edge of clock
 - PLL-based clock regeneration
- ◆ SSTL-2 compatible (2.5V) switching
- ◆ Serial Presence Detect (SPD) EEPROM provides automatic memory configuration
- ◆ Series termination on clock and data lines
- ◆ Board footprint of less than 2.0 square inches
- ◆ Built using thirty-six 256M x 4 DDR SDRAMs, 8K refresh
- ◆ Pin-compatible with all PC1600, PC2100, and PC2700 modules
- ◆ Low Profile: 1.2 inches tall

Selection Guide

CM74SD4096RLP-xxxx/x

MODULE SIZE:
4 GBytes

ADDRESS PATH:
R = Registered

MODULE HEIGHT
LP = 1.2 inches

SPEED:
2700: PC2700 (333 MHz)

RAM VENDOR:
M = Micron
S = Samsung

General Description

The CM74SD4096RLP is a Double Data Rate SDRAM Dual Inline Memory Module (DIMM), designed for applications requiring the ultimate in memory density. This DIMM includes Error Checking and Correcting (ECC) for maximum reliability, and has registered address and control signals to enable fully configured systems.

These modules are constructed using thirty-six 256Mx4 (1024 MBit) DDR SDRAMs in TSOP-II packages, and are fully compliant with appropriate JEDEC specifications. The module also includes an EEPROM to support Serial Presence Detect (SPD) requirements. Decoupling capacitors are mounted on the printed circuit board for each DDR SDRAM device, and series termination is provided on all clock and data lines.

The synchronous design of these Corsair SDRAM DIMMs allows precise cycle control with the use of the system clock. Two I/O transactions are possible on every clock cycle due to the use of double data rate RAMs. The high clock frequency and high density of this device enable a high level of performance to be achieved in advanced workstations and servers.

Pin Definitions

Pin Name	Function
A0 - A13	Address Inputs
BA0, BA1	Bank Address Select Inputs
DQ0 - DQ63	Data Input/Output
CB0 - CB7	ECC Check Bits
DQS0 - DQS17	Data Strobe Input/Output
CK0, /CK0	Clock Inputs
CKE0, CKE1	Clock Enable Inputs
/CS0, /CS1	Chip Select Inputs
/RAS	Row Address Strobe Input
/CAS	Column Address Strobe Input
/WE	Write Enable Input
VDD	Power Supply (2.5V)
VDDQ	Data Input/Output Power Supply
VSS	Ground
VREF	SSTL-2 Signalling Reference Voltage
VDDSPD	Serial EEPROM Power
SDA	SPD Data Output
SCL	SPD Clock Input
SA0 - SA2	SPD Address Inputs
/RESET	Reset Enable
NC	No Connection

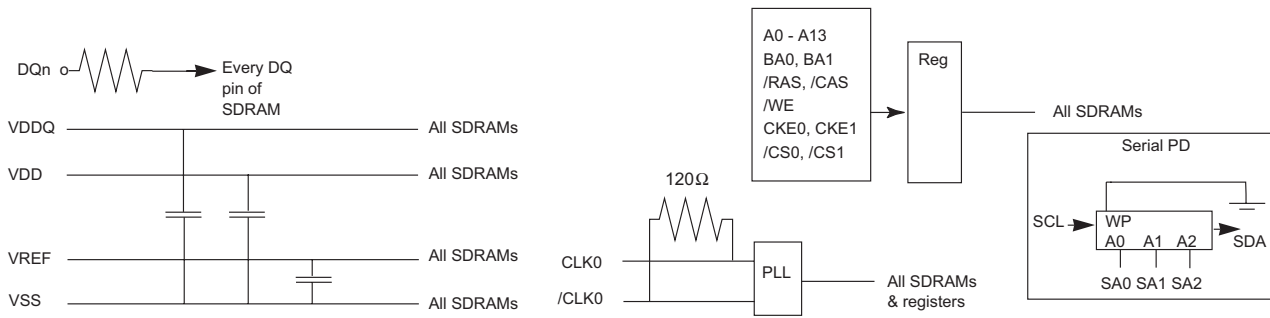
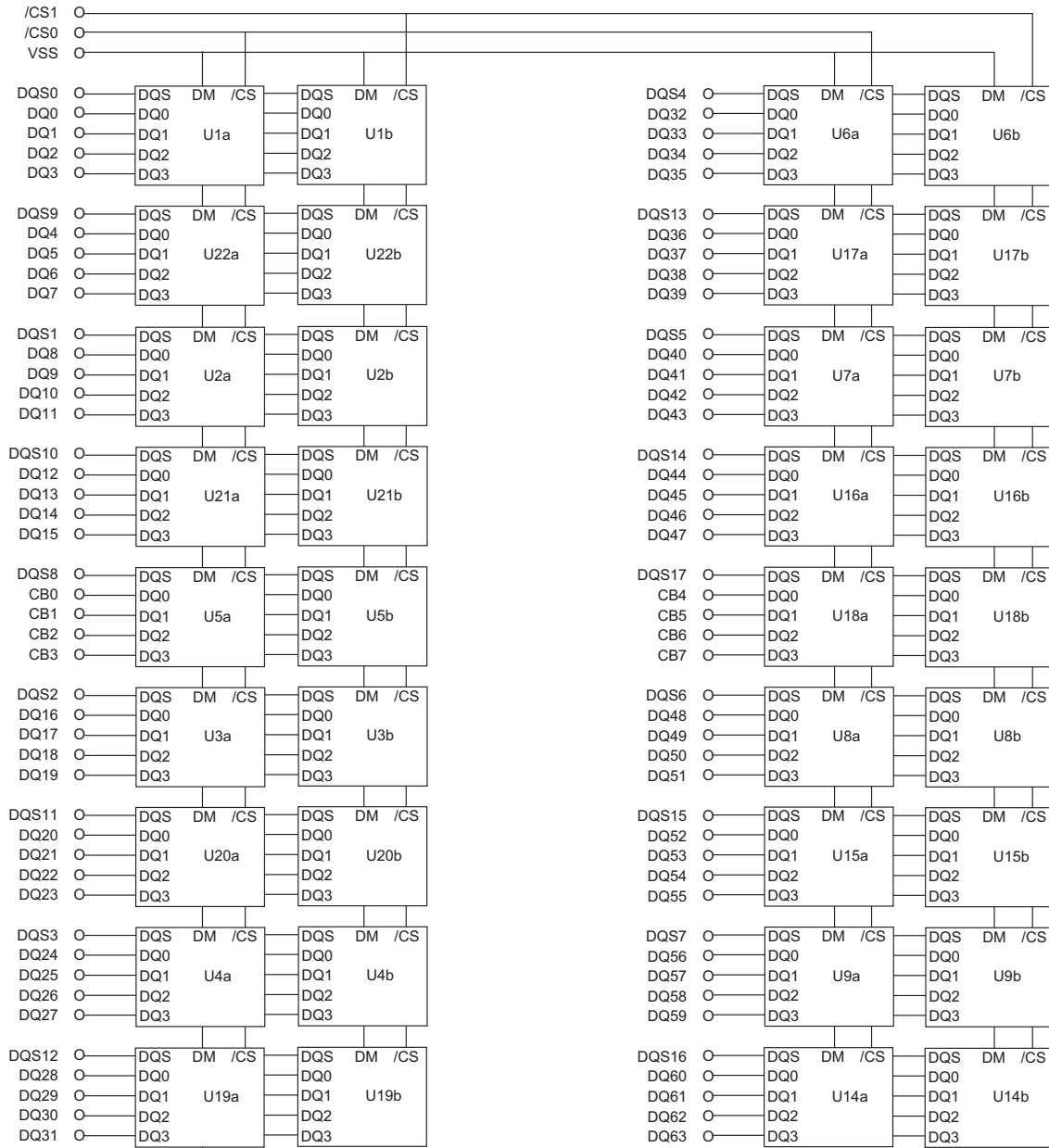


Pin Configuration

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	VREF	93	VSS	47	DQS8	139	VSS
2	DQ0	94	DQ4	48	A0	140	DQS17
3	VSS	95	DQ5	49	CB2	141	A10
4	DQ1	96	VDDQ	50	VSS	142	CB6
5	DQS0	97	DQS9	51	CB3	143	VDDQ
6	DQ2	98	DQ6	52	BA1	144	CB7
7	VDD	99	DQ7	53	DQ32	145	VSS
8	DQ3	100	VSS	54	VDDQ	146	DQ36
9	NC	101	NC	55	DQ33	147	DQ37
10	/RESET	102	NC	56	DQS4	148	VDD
11	VSS	103	NC	57	DQ34	149	DQS13
12	DQ8	104	VDDQ	58	VSS	150	DQ38
13	DQ9	105	DQ12	59	BA0	151	DQ39
14	DQS1	106	DQ13	60	DQ35	152	VSS
15	VDDQ	107	DQS10	61	DQ40	153	DQ44
16	NC	108	VDD	62	VDDQ	154	/RAS
17	NC	109	DQ14	63	/WE	155	DQ45
18	VSS	110	DQ15	64	DQ41	156	VDDQ
19	DQ10	111	CKE1	65	/CAS	157	/CS0
20	DQ11	112	VDDQ	66	VSS	158	/CS1
21	CKE0	113	NC	67	DQS5	159	DQS14
22	VDDQ	114	DQ20	68	DQ42	160	VSS
23	DQ16	115	A12	69	DQ43	161	DQ46
24	DQ17	116	VSS	70	VDD	162	DQ47
25	DQS2	117	DQ21	71	NC	163	NC
26	VSS	118	A11	72	DQ48	164	VDDQ
27	A9	119	DQS11	73	DQ49	165	DQ52
28	DQ18	120	VDD	74	VSS	166	DQ53
29	A7	121	DQ22	75	NC	167	A13
30	VDDQ	122	A8	76	NC	168	VDD
31	DQ19	123	DQ23	77	VDDQ	169	DQS15
32	A5	124	VSS	78	DQS6	170	DQ54
33	DQ24	125	A6	79	DQ50	171	DQ55
34	VSS	126	DQ28	80	DQ51	172	VDDQ
35	DQ25	127	DQ29	81	VSS	173	NC
36	DQS3	128	VDDQ	82	NC	174	DQ60
37	A4	129	DQS12	83	DQ56	175	DQ61
38	VDD	130	A3	84	DQ57	176	VSS
39	DQ26	131	DQ30	85	VDD	177	DQS16
40	DQ27	132	VSS	86	DQS7	178	DQ62
41	A2	133	DQ31	87	DQ58	179	DQ63
42	VSS	134	CB4	88	DQ59	180	VDDQ
43	A1	135	CB5	89	VSS	181	SA0
44	CB0	138	VDDQ	90	NC	182	SA1
45	CB1	137	CK0	91	SDA	183	SA2
46	VDD	138	/CK0	92	SDL	184	VDDSPD



Functional Block Diagram



DC Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on VDD relative to VSS	V _{INVDD}	-1.0 to 3.6	V
Voltage on VDDQ relative to VSS	V _{INVDDQ}	-1.0 to 3.6	V
Voltage on VREF relative to VSS	V _{INVREF}	-0.5 to 3.6	V
Voltage on input pins relative to VSS	V _{IN}	-0.5 to 3.6	V
Voltage on I/O pins relative to VSS	V _{IO}	-0.5 to VDDQ+0.5	V
Storage Temperature	T _{STG}	-55 to 150	°C
Operating Temperature	T _S	0 to 70	°C
Power Dissipation	P _D	36	W
Short Circuit Current	I _{OS}	50	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{DD}	2.3	2.7	V
I/O Supply Voltage	V _{DDQ}	2.3	2.7	V
I/O Reference Voltage	V _{REF}	0.49 x V _{DDQ}	0.51 x V _{DDQ}	V
Input High Voltage	V _{IH}	V _{REF} + 0.15	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	V _{REF} - 0.15	V
Clock Input Voltage	V _{INCK}	-0.3	V _{DDQ} + 0.3	V
Clock Differential Voltage	V _{CKD}	0.3	V _{DDQ} + 0.6	V
Clock Crossing Point Voltage	V _{CKX}	1.15	1.35	V
Input Leakage Current	I _I	-5	5	μA
Output Leakage Current	I _{OZ}	-10	10	μA
Output High Current	I _{OH}	16.8	-	mA
Output Low Current	I _{OL}	-16.8	-	mA

Capacitance

Parameter	Symbol	Max	Unit
Input Capacitance (A0 - A13, BA0 - BA1)	C _{IN1}	11	pF
Input Capacitance (/RAS, /CAS, /WE)	C _{IN2}	11	pF
Input Capacitance (/CS0 - /CS1)	C _{IN3}	11	pF
Input Capacitance (CKE0, CKE1)	C _{IN4}	11	pF
Input Capacitance (CK0, /CK0)	C _{IN5}	12	pF
Input Capacitance (DQS0 - DQS8, DM0 - DM8)	C _{IN6}	16	pF
EEPROM Input Capacitance (SCL, SA0 - SA2)	C _{IN7}	6	pF
I/O Capacitance (DQ0 - DQ63, CB0 - CB7)	C _{IO1}	16	pF
EEPROM I/O Capacitance (SDA)	C _{IO2}	10	pF



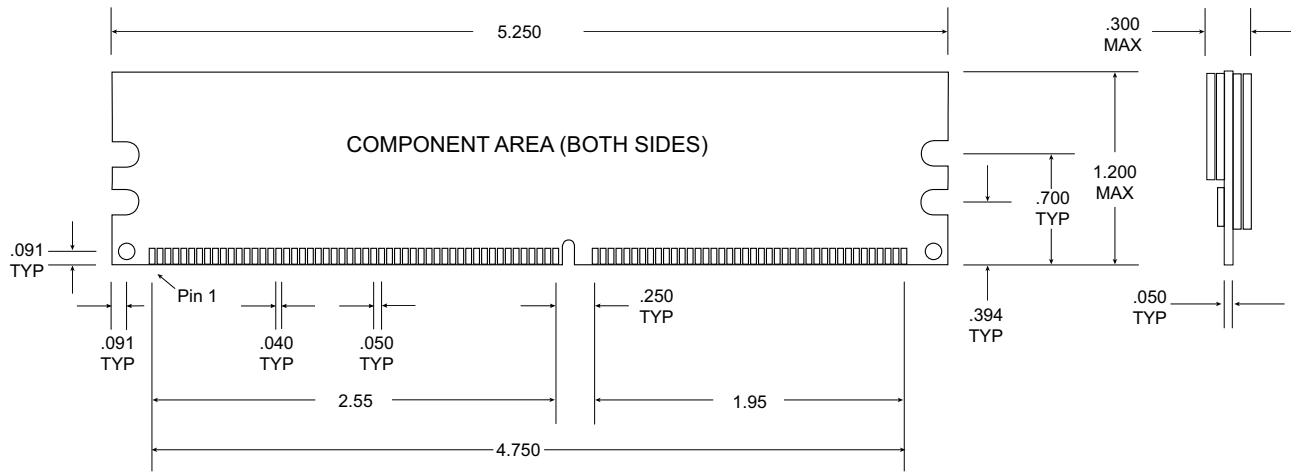
DC Electrical Characteristics

Over the operating range unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current - One bank active precharge	IDD0	tRC = tRCmin; tCK = 133MHz, DQ, DM, and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle		4600	mA
Operating Current - One bank operation	IDD1	One bank; Active-Read-Precharge; Burst = 2; tRC = 133 MHz, CL = 2.5; tCK = tRC = 133 MHz; Iout = 0 mA; Address and control inputs changing once per clock cycle		5140	mA
Precharge Power-Down Standby Current	IDD2P	All banks idle; Power-down mode; CKE = LOW; tCK = 133 MHz		841	mA
Idle Standby Current	IDD2F	/CS = HIGH; All banks idle; CKE = HIGH; tCK = 133MHz; Address and control inputs changing once per clock cycle		2260	mA
Active Power-Down Standby Current	IDD3P	One bank active; Power-down mode; CKE = LOW; tCK = 133 MHz		1705	mA
Active Standby Current	IDD3N	/CS = HIGH; CKE = HIGH; One bank active; Active-precharge; tRC = tRASmax; tCK = 133MHz; DQ, DQM, and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle		3160	mA
Operating Current - Burst Read	IDD4R	Burst length = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; tCK = 133MHz; DQ, DQM, and DQS inputs changing twice per clock cycle		5500	mA
Operating Current - Burst Write	IDD4W	Burst length = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; tCK = 133MHz; DQ, DQM, and DQS inputs changing twice per clock cycle		6760	mA
Auto Refresh Current	IDD5	tRC = tRFCmin		7480	mA
Self Refresh Current	IDD6			913	mA



Package Configuration



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